A Novel Wide-Band Envelope Detector

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***Abstract* — In this paper, we present a novel wide-band envelope detector comprising a fully-differential operational transconductance amplifier (OTA), a full-wave rectifier and a peak detector. To enhance the frequency performance of the envelop detector, we utilize a gyrator-C active inductor load in the OTA for wider bandwidth. Additionally, it is shown that the high-speed rectifier of the envelope detector requires high bias current instead of the sub-threshold bias condition. The experimental results show that the proposed envelope detector can work from 100-Hz to 1.6-GHz with an input dynamic range of 50-dB at 100-Hz and 40-dB at 1.6-GHz, respectively. The envelope detector was fabricated on the TSMC 0.18-um CMOS process with an active area of 0.65^2 mm^2.**

***Index Terms* — Envelope detector, Peak detector, OTA, Rectifier, Gyrator-C active inductor, Wide-band.**

I. Introduction

The envelope detector is extensively applied in the control and energy estimation systems [1]-[3] to track the amplitude of input signals. Recently, many systems require envelope detectors capable of treating with high frequency input signals, such as embedded RFIC test bench [4], AM/ASK receiver and so on. For this reason, this work is dedicated to realize a high-frequency and wide-band envelope detector.

The operation frequency of the conventional envelope detector with op-amp feedback loop is limited by the gain-bandwidth product of the op-amp. This problem can be alleviated by the OTA-rectifier-peak-detector open loop structure as shown in fig.1 [1]. Several envelope detectors based on this configuration have been developed. Benefited from wide linear transconductor, envelope detectors [2] [5] enjoy low power and wide input dynamic range. However, these techniques essentially do not improve the frequency characteristic. The envelope detector proposed in [6] focuses on the trade-off between the keeping and tracking of input signal. Nevertheless, the low-speed circuits included in the envelope detector limit the operation frequency lower than a few hundred MHz.

To further overcome this limitation, the envelop detector proposed in this study employs the gyrator-C active inductor load in the OTA to introduce a zero in the transfer function. Because the zero can compensate the decline of transfer characteristics at the dominant pole, the bandwidth of the OTA is widened. Besides, adopting high bias current in the rectifier improves the operation speed of transistors and hence enhances the frequency performance.

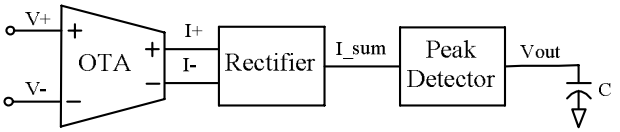

Fig. 1. Envelope detector with OTA-rectifier-peak-detector open loop.

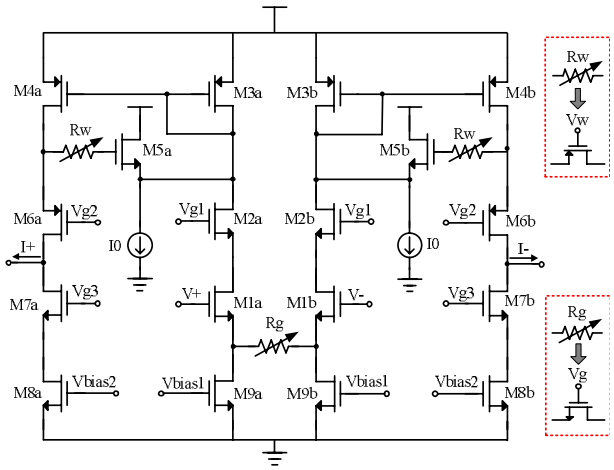

Fig. 2. Schematic diagram of the cascode OTA circuit.

II. Tunable Wide-Band OTA

Fig.2 shows the first stage of the proposed envelop detector, a fully-differential cascode OTA. $M_{4a,b}$, $M_{6a,b}$-$M_{8a,b}$, $M_{5a,b}$, R_w and I_0 constitute gyrator-C active inductor load [7]. The two-port gyrator is mainly formed by the back-to-back connected common-source (CS) amplifier, made up of $M_{4a,b}$ and $M_{6a,b}$-$M_{8a,b}$, and common-drain (CD) amplifier, made up of $M_{5a,b}$ and I_0. One port of the gyrator is connected to the gate-source capacitor of $M_{5a,b}$, hence the other port of the gyrator, the gate of $M_{4a,b}$, exhibits an inductive impedance. To minimize the number of transistors, $M_{4a,b}$ and $M_{6a,b}$-$M_{8a,b}$ are reused as a cascode current mirror. Moreover, the linear range of the OTA is widened through the source degeneration resistor R_g.

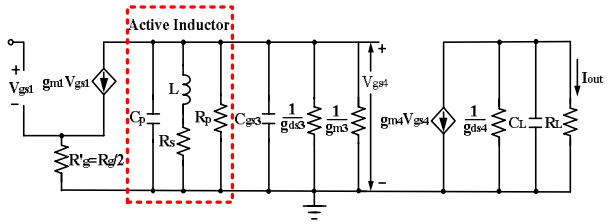

Fig. 3. Small-signal equivalent circuit of the OTA.

The variable resistors R_w and R_g are implemented by triode-region PMOS and NMOS transistors, respectively. They can be adjusted by corresponding voltages V_w and V_g.

Fig.3 shows the small-signal equivalent circuit of the OTA, where the gyrator-C active inductor is modeled as a passive RLC ladder network. Straightforward circuit analysis gives the expressions of L, C_p, R_p and R_s:

$$L = \frac{C_{ds4}(1+R_w g_{ds4})}{g_{m4}g_{m5}}$$

$$C_p = C_{gs4}, R_p \approx \frac{1+R_w g_{ds4}}{g_{m4}}, R_s = \frac{g_{ds4}}{g_{m4}g_{m5}} \quad (1)$$

The g_{mi}, g_{dsi}, and C_{gsi} represent the transconductance, output conductance and gate-source capacitance of corresponding transistors, respectively. Then we can obtain the transfer function of the transconductance $G_m(s)$:

$$G_m(s) \approx \frac{(R_s // 1/g_{m3} // R_p) g_{m1} g_{m4}}{1+g_{m1}R'_g} \cdot \frac{s/(R_s C'_p)+1/(LC'_p)}{s^2+s(R_s/L+1/(R'_p C'_p))+1/(LC'_p)} \cdot \frac{1}{1+s/(R_L C_L)} \quad (2)$$

where $R'_p = R_p||1/g_{ds3}||1/g_{m3}$; $C'_p = C_p + C_{gs3}$; R_L and C_L are resistance and capacitance loads, respectively. Obviously, except for the pole $\omega_{p,l}$ produced by the output node capacitance, the gyrator-C active inductor load contributes a self-resonant frequency point $\omega_{p,s}$ and a zero point ω_z. The $\omega_{p,l}$, $\omega_{p,s}$ and ω_z can be expressed as:

$$\omega_{p,l} = \frac{1}{R_L C_L} \quad (3)$$

$$\omega_{p,s} = \sqrt{\frac{1}{LC'_p}} = \sqrt{\frac{g_{m4}g_{m5}}{C_{gs5}C_{gs4}(1+R_w g_{ds4})}} \quad (4)$$

$$\omega_z = \frac{R_s}{L} = \frac{g_{ds4}}{C_{gs5}(1+R_w g_{ds4})} \quad (5)$$

Observe that the position of $\omega_{p,s}$ and ω_z can be tuned by R_w. Adjust V_w to make $\omega_z<\omega_{p,l}<\omega_{p,s}$. Fig.4 shows the Bode plots of the transfer functions $G_m(j\omega)$ and $G'_m(j\omega)$, where $G'_m(j\omega)$ represents the transfer function of the counterpart without active inductor load. For $G'_m(j\omega)$, $\omega_{p,g}$ stands for the pole point associated with the gate of $M_{3a,b}$, which is

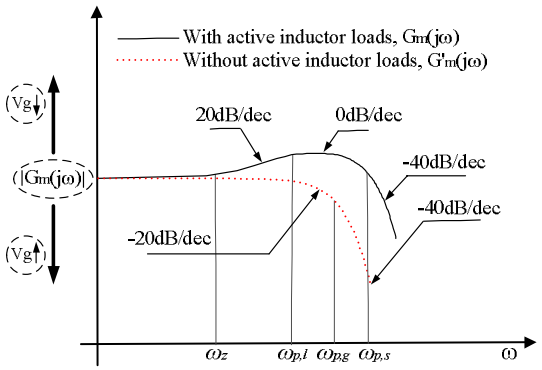

Fig.4. Bode plots of transfer functions $G_m(j\omega)$ and $G'_m(j\omega)$.

assumed to be a little larger than the output pole point $\omega_{p,l}$. In fig.4, we can see the transfer curve of $G_m(j\omega)$ ascends at ω_z by 20dB/dec in advance, as a result, it can successfully eliminate the degradation beyond the output pole point $\omega_{p,l}$ and effectively expand the bandwidth.

Additionally, from (2), we can see the transconductance of the OTA can be tuned by the controllable resistor R_g (see Fig.4).

III. Design of the Full-Wave Rectifier

Fig.5 shows the full-wave rectifier and peak detector circuits. The full-wave rectifier is formed by two half-wave rectifiers consisting of M_{1a}-M_{4a} and M_{1b}-M_{4b}. Acting as a current switch, M_{4a} is initially on the edge of conduction. As the input current $I+$ increases, the voltage at node A (V_A) is driven up. To maintain the fixed drain current of M_{2a} and M_{3a}, the voltages at node B and C (V_B and V_C) significantly decrease. Therefore, M_{4a} is turned off and current $Iout+$ falls to zero. On the contrary, when $I+$ decreases, V_B and V_C rise while V_A drops. Hence M_{4a} turns on and $Iout+$ increases. The output current I_sum flows into the peak detector, which comprises a source follower M_8 and M_9, a storage capacitor C, and a feedback path M_{10} and M_{11}. Because charging current $I1$ of the capacitor is much larger than the discharging current $I2$, the output voltage V_{out} will track the peak value of input signal with only small variations [6].

Ideally, the M_{4a} could be immediately switched on and off as the variation of signal $I+$. Practical, to make M_{4a} switch from the off state to conduction and vice versa, V_A and V_C should experience the swing of ΔV_A and ΔV_C, respectively. Therefore, the output current of the rectifier will exhibit a delay after the zero crossing of the input signal, which can be approximately expressed as:

$$\Delta t = \frac{C_A \Delta V_A + C_C \Delta V_C}{I_{in}}, \quad (6)$$

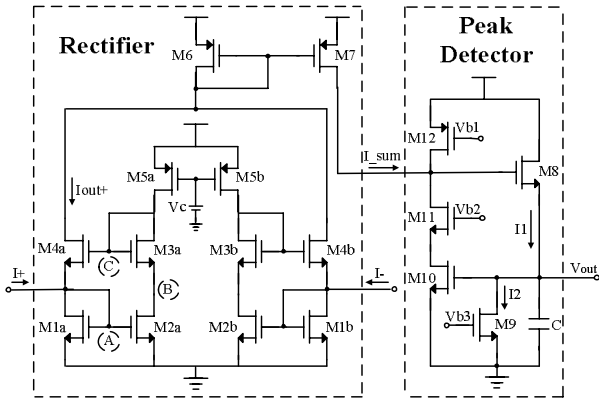

Fig.5. Schematic diagram of the full-wave rectifier and peak detector circuits.

where I_{in} is the input current value of the rectifier, C_A and C_C are capacitances at the node A and C, respectively. If $M_{1a,b}$-$M_{3a,b}$ are biased at sub-threshold region[6][8], V_A and V_C will dramatically depend on the input current. The voltage swings ΔV_A and ΔV_C reach around 0.4V for 400uA input current when $M_{1a,b}$-$M_{3a,b}$ have length and width of 0.18um and 2um, respectively. According to (6), the delay exhibits about 2ns as shown in Fig.6 (a). As the working frequency goes up to 200 MHz, the rectifier can not generate the proper current waveform, which is seen in Fig.6 (b).

To resolve this situation, the node capacitance can be decreased by scaling down the sizes of $M_{1a,b}$-$M_{4a,b}$. Nevertheless, a more effective way is to reduce voltage swings ΔV_A and ΔV_C. To achieve this, we can increase the bias current of $M_{1a,b}$-$M_{3a,b}$ to enhance their transconductance. Meanwhile, in order to keep $M_{4a,b}$ in the sub-threshold region, we should reduce the V_{bias2} of OTA to produce an initial input current slightly smaller than the bias current of $M_{1a,b}$. Consequently, the rectifier with high bias current can reduce its delay by a factor of 10 as shown in Fig.6 (a), which enables the rectifier to work up to GHz. In this condition, M_{1a} can hardly be fully turned off when input current I+ decreases. Therefore, the output current will be smaller than the input current. However, we can increase the transconductance of the OTA in Fig.2 to compensate this current deviation.

IV. Experimental Result

The proposed envelope detector was fabricated on TSMC 0.18-*um* CMOS process. This circuit dissipates 6.3mW with a 1.8-V power supply. Fig.7 shows the chip microphotograph with an active area of 0.65^2 mm^2.

The envelope detector was evaluated using the amplitude modulation signal with a sine-wave carrier and square-wave baseband signal. Fig.8 represents measured input and output voltage waveforms for the input signal

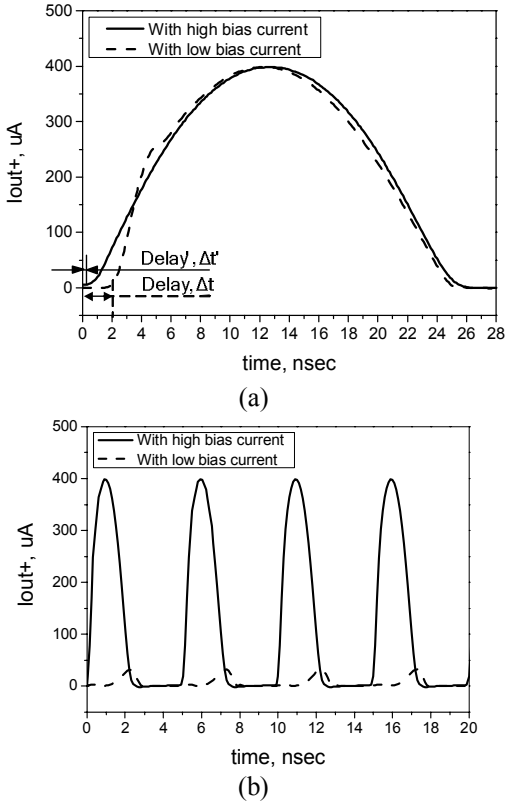

Fig.6. Output current waveform diagram for the rectifier: (a) 20 MHz; (b) 200 MHz.

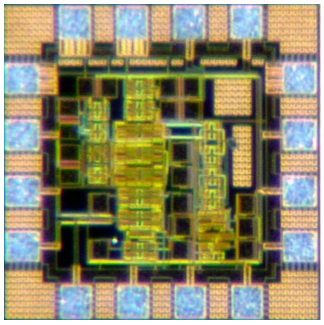

Fig.7. Chip microphotograph of proposed envelope detector.

with 257.5 mV amplitude (A_{mpl}), 500 MHz carrier ($f_{carrier}$) and 5 KHz base-band signal (f_{mod}). We can see that the output voltage exhibits as a 5 KHz, 257.6 mV square wave, successfully tracking the envelope of input signal.

We also checked the input dynamic range over which the envelope detector provides proportional and linear information of the input signal envelope. Fig.9 shows measured transfer characteristics of the envelope detector when $f_{carrier}$ was set to 100 MHz, 500 MHz, 1 GHz and 1.6 GHz, respectively. Accordingly, the envelope detector achieved an input dynamic range of 50 dB, 47 dB, 44.2 dB and 40 dB, respectively.

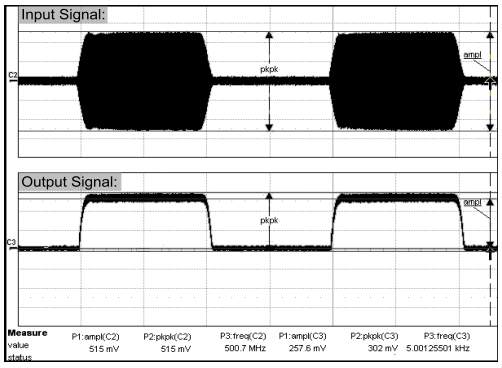

Fig.8. Experimental input and output voltage waveforms on an oscilloscope when A_{mpl} = 257.5 mV , $f_{carrier}$ = 500 MHz and f_{mod} = 5 KHz.

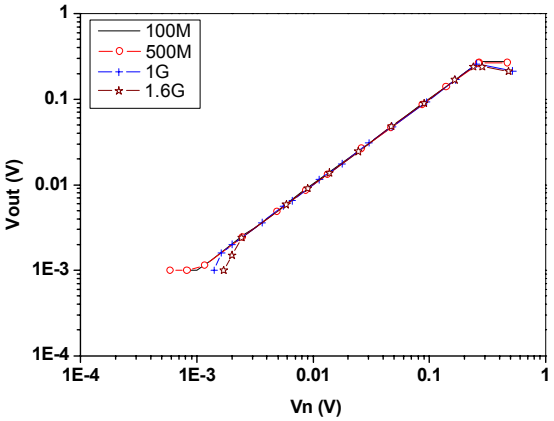

Fig.9. Measured transfer characteristics of the proposed envelope detector when $f_{carrier}$ = 100 MHz, 500 MHz, 1 GHz, and 1.6 GHz, respectively.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work	Ref.[5]	Ref.[6]
Technology	0.18-*um* CMOS	0.15-*um* CMOS	0.35-*um* AMS
Frequency Range	100 Hz ~ 1.6 GHz	100Hz ~ 10 KHz	Up to 0.1 GHz
Input Dynamic Range	40 dB @1.6 GHz	75 dB @10 KHz	Up to 0.3 V @0.1 GHz
Power	6.3 mW	2.8 uW	1.98 mW

Table I summarizes the detailed performance of the proposed envelop detector and compares them with that of representative previous works [5] [6]. Obviously, the proposed envelope detector obtained significant frequency performance improvement with a slightly higher power consumption than the similar circuit in [6], due to the increased bias current of the rectifier.

V. CONCLUSIONS

A wide-band envelop detector consisting of a fully-differential OTA, a full-wave rectifier and a peak detector, has been proposed. Compared with the previous works, the operation frequency of the envelop detector has been significantly improved by employing gyrator-C active inductor load in the OTA and applying high bias current for the rectifier. The proposed envelop detector was simulated and fabricated with TSMC 0.18-*um* CMOS process. Experimental results show that it can work from 100 Hz to 1.6 GHz with the input dynamic range from 50 dB to 40 dB, respectively. This proposed envelope detector enables applications which demand high frequency and wide bandwidth, such as the embedded RFIC test, receiver frond-ends and so on.

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REFERENCES

[1] Michel S. J. Steyaert, Wim Dehaene, Jan Craninckx, Mairtin Walsh, and Peter Real, "A CMOS Rectifier-Integrator for Amplitude Detection in Hard Disk Servo Loops," *IEEE Journal of solid-state circuits.*, vol. 30, no. 7, pp.743-751 , July. 1995.

[2] Michael W. Baker, Serhii Zhak, and Rahul Sarpeshkar, "A MICROPOWER ENVELOPE DETECTOR FOR AUDIO APPLICATIONS," in *Proc. IEEE Intl. Symp. Circuits and Systems.*, vol. 5, May 2003,pp. 1-4.

[3] Chia-Chin Chong, Su Khiong Yong, and Seong Soo Lee, "UWB Direct Chaotic Communication Technology," *IEEE antennas and wireless progagation letters.*, vol. 4, pp. 316-319, 2005.

[4] Donghoon Han, and Abhijit Chatterjee, "Robust Built-In Test of RF ICs Using Envelope Detectors," in *Proceedings of the 14th Asian test symposium.*, 18-21 Dec. 2005, pp.2-7.

[5] Serhii M. Zhak, Michael W. Baker, and Rahul Sarpeshkar, "A Low- Power Wide Dynamic Range Envelope Detector," *IEEE Journal of solid-state circuits.*, vol. 38, no. 10, pp. 1750-1753, Oct. 2003.

[6] J. P. Alegre, S. Celma, M. T. Sanz and P. Martinez, "A Low-Ripple Fast-Settling CMOS Envelope Detector," in *Research in Microelectronics and Electronics 2006, Ph. D.*, pp. 6-12.

[7] Ming-Juei Wu, Jyh-Neng Yang, and Chen-Yi Lee, "A Constant Power Consumption CMOS LC Oscillator Using Improved High-Q Active Inductor with Wide Tuning-Range," in *Circuits and Systems, 2004. MWSCAS' 04. The 2004 47th Midwest Symposium on.*, Vol. 3, 25-28 July 2004, pp. iii-347-50.

[8] Surachet Khucharoensin and Varakorn Kasemsuwan, "A High Performance CMOS Current-Mode Precision Full-Wave Rectifier (PFWR)," in *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on.*, Vol. 1, 25-28 May 2003, pp. 41-44.